

61
Docket Number: 044020-0284163

2826
PATENT APPLICATION

Client Reference: 01F181

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of

SATOSHI INABA

Group Art Unit: 2826

Application No.: 10/042,264

Examiner: Thomas L. DICKEY

Filed: January 11, 2002

Confirmation No.: 6258

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Request is hereby made under Rule 97(d) for consideration of the following IDS for which the requisite \$180 fee under Rule 17(p) is enclosed. Please charge the amount of \$180.00 to our Deposit Account No. 03-3975 under the above Docket Number. Two copies of this paper are attached.

I hereby certify that each enclosed document listed on the herewith Form PTO-1449 was first cited in a communication from a foreign patent office in a counterpart foreign counterpart application in the attached European Communication (Partial Search Report) issued June 30, 2003 i.e., not more than three months ago. See that communication for information on each document.

This IDS is intended to be in full compliance with the rules, but should the Examiner find any part of its required content to have been omitted, prompt notice to that effect is earnestly solicited, along with additional time under Rule 97(f), to enable Applicant to comply fully.

Consideration of the foregoing and enclosures plus the return of a copy

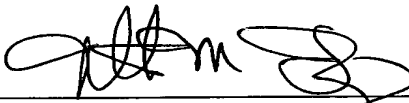
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of the enclosed Form PTO-1449 with the Examiner's initials in the left column per MPEP 609
are earnestly solicited along with an early action on the merits.

Respectfully submitted,


for Dale S. Lazar 37,655
Registration Number 28872

Date: July 29, 2003

PILLSBURY WINTHROP LLP
Telephone: (703) 905-2000
Facsimile: (703) 905-2500
P.O. Box 10500
McLean, VA 22102



Atty. Dkt. No.	M#	Client Ref.
	0284163	01F181

**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**

Applicant: INABA, Satoshi
Appln. No.: 10/042,264
Filing Date: January 11, 2002
Examiner: T. DICKEY
Group Art Unit: 2826

Date: July 29, 2003 Page 1 of 1

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR 5,583,361	12/1996	Morishita			
	BR 5,580,799	12/1996	Funaki			
	CR 4,819,043	04/1989	Yazawa et al.			
	DR					
	ER					
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	HR					
	IR					
	JR					
	KR					
	LR					
	MR					
	NR					

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FOREIGN PATENT DOCUMENTS

	Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract		Translation Readily Available	
						Enclosed	No	Enclose	No
	OR 0 962 988 A2	12/1999	Europe	Higashi et al.		X		X	
	PR 60-50960	03/1985	Japan	Katsuhiko		X			X
	QR 7-335837	12/1995	Japan	Masabumi		X			X
	RR								
	SR								
	TR								
	UR								
	VR								

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

WR	MIYAMOTO et al., "Pseudo-SOI: P-N-P-Channel-Doped Bulk MOSFET for Low-Voltage High Performance Applications," Electron Devices Meeting, 1998, pages 15.3.1-15.3.4			
XR	MIZUNO, Tomohisa, "Analytical Model for High-Performance Shallow-Junction-Well Transistor (SJET) with a Fully Depleted Channel Structure," IEEE Transaction on Electron Devices, vol. 40, no. 1, January 1993, pages 105-111, XP 002240660			
YR				
ZR				

Examiner Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.